

What is claimed is:

1 1. A method comprising:

2 detecting a condition in a processor;

3 calculating adjustment values at stages within a pipeline

4 of the processor; and

5 updating a register with one of the adjustment values

6 when an instruction associated with the condition is

7 terminated within the pipeline.

1 2. The method of claim 1, wherein calculating the adjustment
2 values comprises:

3 incrementing the adjustment values when the condition is
4 detected; and

5 decrementing the adjustment values when the instruction
6 leaves the stages.

1 3. The method of claim 1, wherein detecting a condition
2 comprises detecting an access to a specified memory
3 location.

1 4. The method of claim 1, wherein detecting the condition
2 comprises detecting an instruction within a hardware loop.

1 5. The method of claim 4, wherein detecting the
2 instruction within the hardware loop comprises detecting a
3 bottom match.

1 6. The method of claim 1, wherein detecting a condition
2 comprises detecting a watch point.

1 7. The method of claim 1, wherein updating the register
2 with one of the adjustment values comprises adjusting the
3 register by an amount determined by a counter residing in
4 the stage where the termination occurred.

1 8. The method of claim 1, wherein updating the register
2 comprises updating a speculative register.

1 9. A apparatus comprising:
2 a first register;
3 a second register; and
4 a set of counters to monitor a difference between the
5 first register and the second register.

1 10. The apparatus as in claim 9, wherein the first
2 register is a speculative register and the second register
3 is an architectural register.

1 11. The apparatus as in claim 10, wherein the first
2 register is a speculative count register and the second
3 register is an architectural count register.

1 12. The apparatus as in claim 9, wherein the first
2 register, second register and set of counters reside in a
3 multi-stage pipeline controlled by a control unit, and the
4 set of counters include counters maintained at a stage
5 where the first register resides and at stages after the
6 stage where the first register resides.

1 13. The apparatus as in claim 12, wherein the set of
2 counters consist of counters residing at stages before an
3 n^{th} stage of a pipeline, and wherein n defines a point at
4 which allowing instructions to flow through the pipeline
5 takes an amount of time less than or equal to a branch
6 penalty.

1 14. The apparatus as in claim 12, wherein following a
2 termination of an instruction in the pipeline, the control
3 unit is adapted to adjust the first register by an amount
4 determined by a particular counter maintained in a stage
5 where the termination occurred.

1 15. The apparatus as in claim 12, wherein the control unit
2 is adapted to:

3 increment the counters when the first register is
4 adjusted because of a detected condition; and

5 decrement a respective counter when the instruction
6 leaves a respective stage associated with the respective
7 counter.

1 16. A system comprising:

2 a static random access memory device;

3 a first register;

4 a second register;

5 a set of counters; and

6 a processor coupled to the static random access memory
7 device, wherein the processor includes an execution
8 pipeline and a control unit adapted to:

9 increment the counters when the first register is
10 adjusted because of a detected condition; and

11 decrement a respective counter when the
12 instruction leaves a respective stage of the pipeline
13 associated with the respective counter.

1 17. The system of claim 16, wherein following a
2 termination of the pipeline, the control unit is adapted to
3 adjust the first register.

1 18. The system of claim 17, wherein control unit is
2 adapted to adjust the first register by an amount
3 determined by one of the set of counters.

1 19. The system of claim 18, wherein the one of the set of
2 counters is a particular counter residing in a stage of the
3 pipeline where the termination occurred.

1 20. The system of claim 17, wherein the control unit is
2 adapted to drain unaborted instructions and write the first
3 register with the data in the second register, if the
4 termination occurs in a stage of the pipeline after an n^{th}
5 stage.